

Can You Really Build a System-on-a-Chip in 90 Days?

VLSI Technology believes that "the best way to develop custom silicon is to start with proven, working silicon."

by
Murray
Shohat

VLSI Technology, Inc. (San Jose) is boldly staking a claim to provide the shortest times to revenue for multimillion-transistor custom ICs. In the works for more than a year, the company's Velocity rapid silicon prototyping (RSP) program implements the equivalent of a hard intellectual property (IP) smorgasbord on a single chip. To arrive at silicon in record time—perhaps 12 weeks or less—design engineers "deconfigure" the chip with a

new VLSI-developed EDA tool: the Hardware Description Language Integrator, or HDLI, which is compatible with normal EDA tool flows.

Citing the growing design productivity gap as the motivating force behind Velocity's development, VLSI's Senior Vice President Bob Payne argues that "the current software-dominated design style is running a losing race against Moore's law." To bridge the gap, new ways must be found to leverage the design

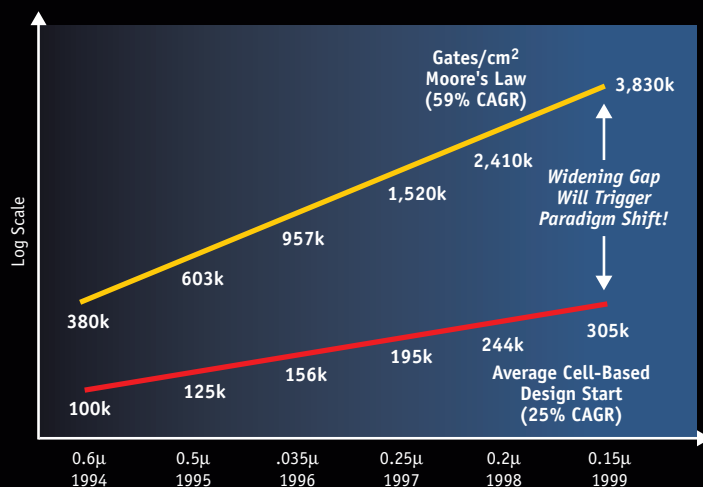
cycle (see Figure 1). VLSI's answer is RSP. At the most fundamental level, it "puts into practice our belief that the best way to develop custom silicon is to start with proven, working silicon," declares Payne.

VLSI's way sounds radical, but like many good ideas it is also obvious. The working silicon isn't merely a collection of characterized hard IP cores for CPU, memory, glue logic, I/O, and the like—all to be assembled into a system on a chip (SOC) over a normal design cycle spanning 6 to 18 months. VLSI has crafted an aggressive package beginning with a sophisticated, tested, highly resourced SOC (in a 456-pin enhanced plastic ball grid array) called the Velocity RSP7. Spanning nearly 200,000 logic gates, with ample SRAM and ROM, it employs high-speed buses in silicon for both deconfiguration and customization. These buses provide the architectural basis for design reuse.

Although the initial offering employs 0.35- μ m design rules, VLSI is now moving into very deep submicron territory for its PCI-enabled version, the RSP7pci, due next year. To achieve the desired functional characteristics, reports Mark Bapst, director of engineering for strategic technology, VLSI is using advanced EDA products, including several VDSM tools from Avant! Corp. (Fremont, CA) to prepare the reference

Figure 1

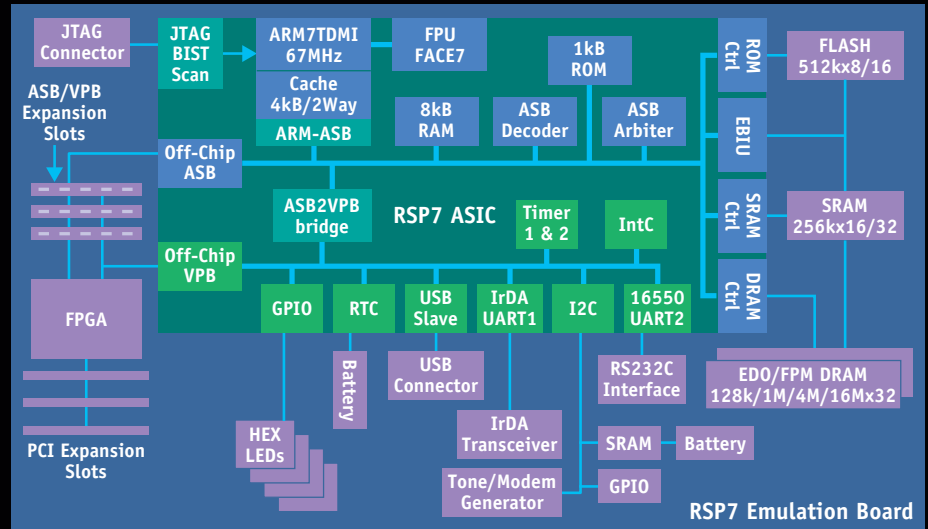
Design Productivity Gap



The worldwide IC industry has always been capable of manufacturing more than it can design. But the gap is widening thanks to larger wafers, increasing manufacturing automation, and the design difficulties of products with very high gate counts. VLSI's Velocity may trigger a paradigm shift by drastically shortening the design cycle. (Source: VLSI Technology)

Figure 2

Velocity RSP7 Development Platform



*ASB & VPB are AMBA Compliant

VLSI's development environment includes the prototype RSP7 chip, a development-board-level platform, and the HDL design automation software. The company's longer-range platform roadmap generally follows the plan for ARM RISC processors from Advanced RISC Machines and VLSI's mixed RISC-DSP plan. This development platform surrounds the RSP7 chip, whose heart is the Advanced RISC Machines ARM7 67-MHz microprocessor with a 4-kbyte, two-way cache. (Source: VLSI Technology)

design (see "Avant! Tools Play a Key Role in Velocity").

Simultaneous Development

The first major difference engineers and managers notice when they compare Velocity with other SOC approaches may be the parallel development of system hardware and software. By starting out with working, characterized silicon, the Velocity program doesn't hold the software team at bay until chips arrive from the foundry.

As a hardware/software co-development vehicle, the RSP7 contains many more features and circuit blocks than typical SOC applications require. Deconfiguration is the act of removing IP blocks; customization allows customer-specific circuits to be developed and installed in the RSP chip as IP blocks. Existing blocks can also be modified rather than deconfigured, adding more market differentiation to the mix of design capabilities.

To bring the Velocity concept to market, VLSI created a development environment consisting of the prototype chip family, a development-board-level platform, and the HDL design automation software. It has also defined a longer-range platform road map that generally follows the plan for ARM RISC processors from Advanced RISC Machines, Ltd. (Cambridge, U.K.) and VLSI's mixed RISC-

DSP plan. This development platform surrounds the RSP7 chip (see Figure 2).

At the chip's heart is the venerable and popular Advanced RISC Machines ARM7 67-MHz microprocessor with a 4-kbyte, two-way cache, as well as the industry-standard AMBA (Advanced Microcontroller Bus Architecture) system bus (ASB) interconnecting the required resources and system controls. A bridge to a second on-chip bus—the VLSI peripheral bus (VPB), also an ARM-driven de facto standard—makes it possible to remove, modify, or replace deconfigurable IP blocks with customer-specific functions built with HDL tools. Both buses are ported off chip to expansion slots on the ATX-like board-level platform. These buses imple-

ment nearly unlimited functionality during development (see Figure 3).

VLSI's use of buses foreshadows current attempts at industry standardization for the same purpose. But while the On-Chip Bus (OCB) Committee of the Virtual Socket Interface Alliance (VSIA) publishes indecisive papers, VLSI is fielding standards-based buses that "make sense for our business," remarks Ed Rocha, the company's director of marketing for strategic technology. "The buses we are using conform to the corporate processor—ARM—and business needs [PCI] of VLSI." Rocha thinks the VSIA's OCB effort faces much greater difficulty because one of its aims is transparent interoperability for IP

Avant! Tools Play a Key Role in Velocity

The Velocity silicon roadmap is now entering the arena of very deep submicron geometry. To prepare deconfigurable reference chips with features down to 0.2 μm , VLSI Technology is using a wide variety of EDA tools, together with the firm's own HDL Integrator (HDLi) IP delivery tool. Avant! tools being used in the program include the following:

- Milkyway, a database and common graphical user interface solution that optimizes multiple domains of design tasks, ranging from floorplanning, very deep submicron optimization, physical and timing analysis, parasitic extraction, layout editing, and physical verification.
- Apollo, a Milkyway-related cell-based VDSM place-and-route system.
- The Hercules hierarchical physical-design verification tool.

from different vendors, an approach that requires an impractical menu of buses.

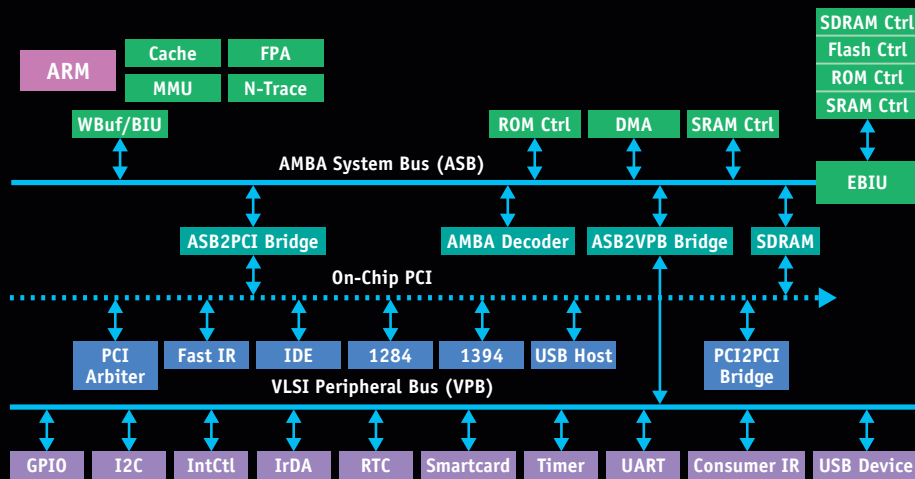
When the ubiquitous PCI bus in the next revision of VLSI's Velocity offering adds even more I/O capabilities (see Figure 3), Velocity will gain appeal for embedded applications as VLSI pushes the technology into the very deep submicron realm. Later, after VLSI adds DSP IP to

the reference design, the gates will open wide to applications as diverse as industrial automation motion control and a broad array of digital consumer goods. Customers for the inaugural version of Velocity are coming from the same markets that find the ARM processor attractive. "The market space is unlimited!" says Rocha. "Anyone desiring a flexible processor solution with a design style that sharply reduces their time to market is a potential customer." ARM is a silver bullet solution for such markets as wireless communications (cell phones and wireless LANs), networking (LANs and WANs), consumer digital products, and advanced computing products like workstations, embedded automation equipment, storage systems, and data security.

ARM and DSP are VLSI's processor cores, but Rocha notes that "others can be used. We currently have a design using RSP7 and an Intel x86 processor; the other IP was the critical factor for time to market—not the CPU. The available IP and ability to quickly customize are by far more important."

Figure 3

On-Chip Buses



The industry-standard AMBA system bus (ASB) interconnects the required resources and system controls. A bridge to a second on-chip bus—the VLSI Peripheral Bus (VPB), also an ARM-driven de facto standard—makes it possible to remove, modify, or replace deconfigurable IP blocks with customer-specific functions built with HDLi tools. These buses, both ported off chip to expansion slots on the ATX-like board-level platform, implement almost unlimited functionality during development. VLSI is now moving into very deep submicron territory for its PCI-enabled version of the prototype chip, the RSP7pci, due next year. (Source: VLSI Technology)

View from the Benchtop

Development engineers in the Velocity environment work with a system that includes VLSI's RSP7 deconfigurable ASIC, an FPGA (the popular 100,000-gate

Figure 4

Deconfiguration: The Essence of Velocity

Gatefield), an emulation board, software drivers, the VxWorks board-support package, the Jumpstart ARM integrated development environment, JTAG-debug, and documentation. Expansion slots are provided for both ASB/VPB-based and PCI boards. Other resources include 256-kbyte x 32-bit SRAM, 512-kbyte x 16-bit flash, 32-Mbyte x 32-bit EDO DRAM, and communications facilities (RS232, USB, IrDA, and GPIO). Board space is also allocated for wire-wrap activity. Designers can add or subtract logic blocks in the prototype ASIC with HDLi, which runs on either Solaris 2.X (SunOS 5.X) or HP-UX 9.X/10.X and supports Verilog and VHDL design flows with synthesis scripts, a test bench, and automated documentation. Physical designs are provided for hard IP.

For simple systems, deconfiguring existing blocks gives customers the shortest time to silicon—as soon as 12 weeks, VLSI believes, and less as the program matures in the hands of customers (see Figure 4). The company's initial RSP7 chip took 18 weeks, but the firm admits that it intentionally selected a "green" engineer to design it.

Of course, custom efforts using third-party IP will take longer, but HDLi software eases the road to integration. After the deconfiguration stage, HDLi is used again to optimize the design for volume production. When the designers arrive at the

final specification, they run the HDL code through their conventional EDA tool chain to floor-plan the back end, route signals, design the packaging, check design rules, and undertake general verification. The chain produces a netlist (GDS-II tape) that goes back to VLSI's fab for manufacturing.

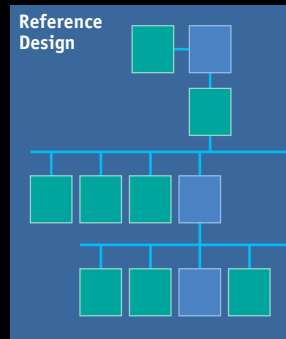
If all this happens in 12 weeks—or even 20—VLSI will surely have succeeded in shifting the paradigm of design styles. Such fast silicon suggests that RSP7 could be used at the same time to develop market-driven roadmap parts, which add features and offer time-to-price-point capabilities using a common reference design. In fact, each successful modification of an RSP reference chip results in a new reference chip. As customers come on board, a swelling reference library of readily reusable IP will make Velocity increasingly

attractive. Customers range from completely independent fabless IC developers to system organizations that want VLSI to handle the design work to their requirements.

Velocity could catch fire, VLSI hopes, as an incredibly good idea. The company claims to have a number of beta-site designs under way; in fact, they may be finished and on the market by the time you read this article. If imitation is really the sincerest form of flattery, can other deconfigurable smorgasbord chips from VLSI's competitors be far behind?

Murry Shohat is a freelance technology writer based in Santa Rosa, CA.

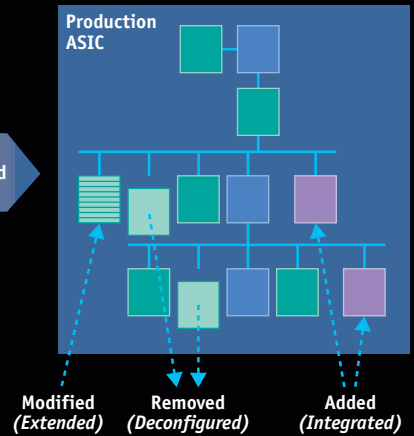
Deconfigurable & Extendible
Prototype Chip Made from
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■ VLSI IP
■ Third Party IP
■ Customer IP

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