

## Reducing the Cost of Wireless LAN Chipsets

*Dual-band WLAN chipset cost can be reduced by integrating a MAC/modem, Zero-IF CMOS radio.*

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There is little doubt that the wireless Local Area Network (WLAN) market is migrating from 802.11b products to solutions offering faster transmission speeds on bands with less interference. The main contenders are 802.11a WLAN products featuring transmission speeds up to five times higher (54 Mbps compared to 11 Mbps for 802.11b), more channel capacity (twelve channels compared to three), and superior reliability on the uncrowded 5 GHz UNII band.

Another proposed IEEE 802.11 standard, 802.11g, offers transmission speeds comparable to 802.11a while offering backward-compatibility with the 802.11b network products. Unfortunately, 802.11g runs on the same cluttered 2.4 MHz ISM band and exhibits the same channel capacity as does 802.11b.

While the industry sorts out standards and users ponder over choices, WLAN chipset manufacturers are developing dual-band wireless solutions compatible with both the 2.4 GHz and 5 GHz bandwidths. As dual-band solutions offer the advantages of speed, capacity, security, and backward compatibility with the installed base of 802.11b products, they are expected to comprise the majority of WLAN product shipments in the future.

Wireless network equipment vendors who can deliver cost-effective dual-band products using these new chipsets will have a definite competitive advantage. One way design engineers can reduce the cost of their dual-band WLAN solutions is by carefully addressing the underlying chipset architecture, especially the integration of the modem and Media Access Controller (MAC) and the type of radio transceiver architecture used.

### Dual-Band Chipset Building Blocks

To be compatible with 802.11a/b/g standards, WLAN chipsets must support both Orthogonal Frequency Device Multiplexing (OFDM) modulation used by the 802.11a and 802.11g standards and Complementary Code Keying (CCK) modulation used by 802.11b products running at 2.4 GHz. In a dual-band client configuration such as a PC card, the dual-band chipset operates in only one standard at a time. The MAC periodically scans both bands for an available channel and the system makes the decision on which channel to initiate communication, similar to the way a client scan is performed in a single-band device.

A conventional dual-band chipset consists of three building blocks: a radio subsystem with dual transceiver capabilities for both the 5 GHz and 2.4 GHz bands, a modem that supports both CCK and OFDM modulations, and a unified MAC supporting all three 802.11 standards. Many first generation dual-band chipsets will be offered in this multiple-chip architecture.

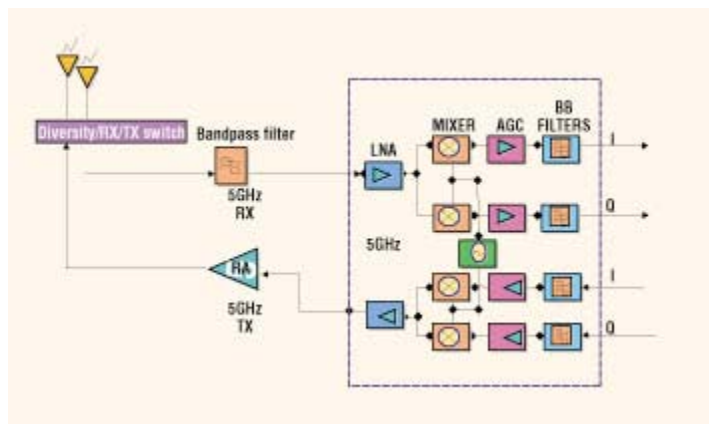
Alternatively, Resonext has developed a solution that significantly reduces the cost of dual-band chipsets through the use of extensive integration and the implementation of a zero-IF radio transceiver on CMOS. These innovations enable its RN5220 dual-band chipset architecture based on a two-chip CMOS solution.

To reduce costs in a dual-band chipset, the OFDM and CCK modems can be designed using dedicated hard-wired DSP engines for each modulation scheme, or implemented via an embedded programmable DSP processor, or with a combination of the two designs. Selecting the right MAC architectures is also an important cost-reduction factor. As with any component, a MAC's flexibility, performance, and power consumption must all be taken into consideration. Resonext has found that the 802.11 MAC is best implemented in software running on an on-chip embedded processor, with the addition of MAC acceleration hardware. This software MAC has the flexibility to support 802.11a, 802.11b, and 802.11g protocols, as well as the IEEE Quality of Service (QoS) and the emerging security standards. In addition, a MAC designed to support 54 Mbps for 802.11a can easily support the lower 11 Mbps data rates of an 802.11b WLAN product as well as the emerging 802.11g based solution.

### Dual Band Zero-IF CMOS Radio Transceiver Cuts Cost

The main cost-reduction factor in dual-band chipsets is the architecture of the radio transceiver, since conventional radio techniques, such as the dual conversion (or superheterodyne) approach, would typically require the implementation of multiple RF chips to support the dual 2.4 GHz and 5 GHz bands. Resonext chose direct conversion, or a zero-Intermediate Frequency (IF) radio transceiver, on standard CMOS process as the architecture of choice for its dual-band RF design. The zero-IF radio utilizes one mixer stage to convert the desired signal directly to and from the baseband without any intermediate IF stages and without the need for external components such as Surface Acoustic Wave (SAW) filters. The Low Noise Amplifier (LNA), Mixers, Voltage Controlled Oscillator (VCO), Synthesizers, and the baseband filters can also be integrated into the chip.

A major advantage of zero-IF architecture on CMOS is that it enables the implementation of a full transceiver on a monolithic die. For the company's first 5 GHz design shown in Figure 1, the receiver section is at the upper top portion of the RF transceiver block diagram.



**Figure 1.**

The desired received signal enters the RF chip from the antenna through an external bandpass filter which passes the entire desired frequency band while rejecting all other undesired frequencies.

The first block the signal encounters inside the chip is the Low Noise Amplifier (LNA), which

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amplifies the receiving signal (from noise) to be processed in the subsequent stages. After the LNA stage, the direct conversion mixer translates the desired signal all the way to baseband frequency by multiplying the input signal with a Local Oscillator (LO).

The output of the mixer stage is sent in quadrature (I and Q channels) to the Automatic Gain Control (AGC) amplifier stage. The AGC provides the attenuation of in-band undesirable signals and ensures the correct signal levels are fed to the baseband processor. At this point, the signal goes through baseband filters which prevent the signal from saturating the receive Analog to Digital Converter (ADC) in the baseband IC.

The transmitter operates similar to the receiver, except in reverse direction. The transmitter starts with the I and Q inputs from the baseband chip and is "up-converted" via a mixer stage driven by the same LO as the receiver structure. The outgoing signal then goes through an on-chip amplifier driver before exiting the RF chip to the input of an external Power Amplifier (PA).

Zero-IF CMOS architecture does present some engineering challenges, such as DC offset, flicker noise, and LO pulling. DC offsets are generated mainly by LO leakage, which self mixes, thereby creating a DC component in the signal chain. This can affect receiver performance and cause the RF stages to saturate. Flicker noise, also known as 1/f noise, is low-frequency device noise that can corrupt signals in the receiver chain. Flicker noise is more pronounced with the CMOS Zero-IF architecture because of the direct conversion to low-frequency baseband. Finally, the pulling of the LO by the PA output affects direct up-conversion process because the high-power PA output, which has a spectrum centered around the LO frequency, can disturb ("pull") the transmitter VCO itself.

Fortunately, recent advances in radio and modem designs, coupled with monolithic CMOS techniques, are able to resolve these issues through a combination of proprietary radio design techniques and system algorithms in the baseband. For example, flicker noise can be handled by transistor tuning in the radio chip and DC offset can be addressed using a compensation scheme in which the offset is measured and reduced through a unique radio and baseband algorithm. Today, direct conversion radios are widely used in cellular phone and pager applications and are increasingly appearing in WLAN radio designs.

After developing a single chip 5 GHz zero-IF radio for its first product, Resonext developed a single chip dual-band 802.11a/b/g radio by combining the 5 GHz and 2.4 GHz zero-IF transceiver structures into a single dual-band radio built on CMOS. Due to the simplicity of the conversion scheme, the 2.4 GHz and 5 GHz zero-IF transceiver circuitry can be laid side by side on a monolithic die without much impact to the die size or package cost and without additional external components, such as SAW filters. Coupled with an integrated dual band modem/ MAC chip, this radio enables a cost effective 2 chip dual band chipset solution.

### **Two-Chip Solution Lowers BOM Costs**

The bottom line savings of a two-chip solution using the direct conversion radio are considerable. Assuming that the superheterodyne dual-conversion chipset and a zero-IF direct-conversion chipset are priced the same, the zero-IF delivers a cost savings of approximately 10 percent on the bill of materials and a space savings of over 50 percent on the PCB area.

Although both radio architectures would still need distinct front-end subsystems (the

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diversity antenna, diversity switches, RX/TX switches, low pass filters, and PAs) due to the impedance matching requirements of the 2.4 GHz and 5 GHz paths, in the future, these functions could be combined through the use of silicon or package integration. For example, just as the PA/switch combo is available today for a single-band system, the 2.4 GHz PA and the 5 GHz PA could be combined into a single chip along with the switches.

Ultimately, the cost of the final dual-band WLAN system is determined by the cost structure of the underlying chipset architecture. Cost reduction in the modem and MAC portions of dual-band chipsets can be achieved through silicon integration. The most cost effective dual-band chipset architecture will have an integrated OFDM modem, CCK modem, and a unified MAC that supports the 802.11a and 802.11b standards, as well as the upcoming 802.11g standards. In addition, design engineers should pay special attention to the various radio architectures being employed today, as it is the RF portion of the chipset that has the largest impact on the cost of the entire system design. Ultimately, the lowest cost chipset architecture will employ the most integrated radio design approach.

For more information contact Resonext Communications, Inc., by calling 408-436-3939 or visit Resonext on the web at [www.resonext.com](http://www.resonext.com).

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